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EXAMINER	
KNOLL, CLIFFORD H	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,472	JAMES ET AL.	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *11/24/04*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 8/30/04. Currently claims 1-51 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. *Claims 1, 6-10, 14-15, 20-22, 26, 31-35, 38-39, 44-46, 49 are rejected under 35 U.S.C. 102(b) as being anticipated by Colmenero (US 4365245).*

Regarding claim 1, Colmenero discloses automatically determining whether an external component is connected to the first port and identifying as active or inactive thereby (e.g., col. 4, lines 28-34), and distinguishing between active and inactive ports during control (e.g., col. 3, lines 60-68).

Regarding claim 6, Colmenero also discloses controlling identified active ports (e.g., col. 3, lines 22-25).

Regarding claim 7, Colmenero also discloses sequencing only identified active ports (e.g., col. 4, lines 44-48).

Regarding claims 8 and 9, Colmenero also discloses the external port as an open or closed circuits (e.g., col. 4, lines 49-55).

Regarding claim 10, Colmenero also discloses the external component corresponds to a length of wire (e.g., col. 4, lines 49-55).

Regarding claim 14, Colmenero discloses automatically identifying active ports, which are those with an external load physically connected (e.g., col. 4, lines 49-55), and sequencing only desired active ports of the electronic device (e.g., col. 4, lines 23-28).

Regarding claim 15, Colmenero also discloses identifying non-active ports of the electronic device, which are not physically connected to an external load and ignoring non-active ports in sequencing operations (e.g., col. 4, lines 23-25).

Regarding claims 20 and 21, Colmenero also discloses the external port as an open or closed circuits (e.g., col. 4, lines 49-55).

Regarding claim 22, Colmenero also discloses the external component corresponds to a length of wire (e.g., col. 4, lines 49-55).

Regarding claim 26, Colmenero discloses a processor and memory (e.g., Figure 1, "56", "40"), the system configured or designed to automatically determine whether an external component is connected to the first port (e.g., col. 4, lines 28-34), and the system designed to distinguish between active and inactive ports during management (e.g., col. 3, lines 60-68).

Regarding claim 31, Colmenero also discloses controlling identified active ports (e.g., col. 3, lines 22-25).

Regarding claim 32, Colmenero also discloses sequencing only identified active ports (e.g., col. 4, lines 44-48).

Regarding claims 33 and 34, Colmenero also discloses the external port as an open or closed circuits (e.g., col. 4, lines 49-55).

Regarding claim 35, Colmenero also discloses the external component corresponds to a length of wire (e.g., col. 4, lines 49-55).

Regarding claim 38, Colmenero discloses a processor and memory (e.g., Figure 1, "56", "40"), a sequencing system configured or designed to automatically determine whether an external component is connected to the active ports (e.g., col. 4, lines 28-34), and the system designed to sequence only active ports during management (e.g., col. 3, lines 60-68).

Regarding claim 39, Colmenero also discloses automatically identifying non-active ports, which are those with an external load not physically connected (e.g., col. 4, lines 49-55), and a configuration to ignore non-active ports (e.g., col. 4, lines 23-28).

Regarding claims 44 and 45, Colmenero also discloses the external port as an open or closed circuits (e.g., col. 4, lines 49-55).

Regarding claim 46, Colmenero also discloses the external component corresponds to a length of wire (e.g., col. 4, lines 49-55).

Regarding claim 49, Colmenero also discloses an active port detection circuit configured to automatically identify active ports (e.g., col. 3, lines 19-22). The automatic identification of Colmenero is engendered by the presence of an active port as disclosed (col. 4, lines 44-49).

2. *Claims 1-3, 5-10, 13-15, 17, 19-22, 25, 26, 28, 30-35, 38, 39, 41, 43-46, 49-51 are rejected under 35 U.S.C. 102(e) as being anticipated by McAlear (US 6697372).*

Regarding claim 1, McAlear discloses automatically determining whether an external component is connected to the first port and identifying as active or inactive thereby (e.g., col. 2, lines 64-66), and distinguishing between active and inactive ports during control (e.g., col. 3, lines 13-20).

Regarding claim 3, McAlear also discloses detection of a resistive load (e.g., col. 2, lines 64-66).

Regarding claim 5, McAlear also discloses detecting the presence of a current flowing and identifying thereby (e.g., col. 2, lines 64-66).

Regarding claim 6, McAlear also discloses controlling identified active ports (e.g., col. 3, lines 13-20).

Regarding claim 7, McAlear also discloses a sequencer; sequencing only identified active ports of the device (e.g., col. 3, lines 39-41).

Regarding claims 8 and 9, McAlear also discloses open and closed circuits (e.g., col. 2, lines 64-66).

Regarding claim 10, McAlear also discloses the length of wire (e.g., col. 2, lines 64-66, "current flowing").

Regarding claim 13, McAlear also discloses the computer program product of the parent claim (e.g., col. 2, line 28-30, "USB host software").

Regarding claim 14, McAlear discloses automatically identifying active ports characterized by external load (e.g., col. 2, lines 64-66), and sequencing only desired active ports of the electronic device (e.g., col. 3, lines 39-41).

Regarding claim 15, McAlear also discloses identifying non-active ports characterized by a port not physically connected (e.g., col. 3, lines 19-20).

Regarding claim 17, McAlear also discloses response to a resistive load (e.g., col. 2, lines 64-66).

Regarding claim 19, McAlear also discloses detecting the presence of a current flowing and identifying thereby (e.g., col. 2, lines 64-66).

Regarding claims 20 and 21, McAlear also discloses open and closed circuits (e.g., col. 2, lines 64-66).

Regarding claim 22, McAlear also discloses the length of wire (e.g., col. 2, lines 64-66, "current flowing").

Regarding claim 25, McAlear also discloses the computer program product of parent claim (e.g., col. 2, line 28-30, "USB host software").

Regarding claim 26, McAlear discloses memory and processor (e.g., col. 2, lines 28-30), system automatically determines whether an external component is connected and identifies as active or inactive (e.g., col. 2, lines 64-66), and distinguishing between active and inactive ports (e.g., col. 3, lines 13-20).

Regarding claim 28, McAlear also discloses response to a resistive load (e.g., col. 2, lines 64-66).

Regarding claim 30, McAlear also discloses detecting the presence of a current flowing and identifying thereby (e.g., col. 2, lines 64-66).

Regarding claim 31, McAlear also discloses controlling identified active ports (e.g., col. 3, lines 13-20).

Regarding claim 32, McAlear also discloses sequencing only active ports (e.g., col. 3, lines 39-41).

Regarding claims 33 and 34, McAlear also discloses open and closed circuits (e.g., col. 2, lines 64-66).

Regarding claim 35, McAlear also discloses the length of wire (e.g., col. 2, lines 64-66, "current flowing").

Regarding claim 38, McAlear discloses memory and processor (e.g., col. 2, lines 28-30), system automatically determines whether an external component is connected and identifies as active or inactive (e.g., col. 2, lines 64-66), and sequencing only active ports (e.g., col. 3, lines 39-41).

Regarding claim 39, McAlear also discloses identifying non-active ports and ignoring non-active ports (e.g., col. 3, lines 39-41).

Regarding claim 41, McAlear also discloses response to a resistive load (e.g., col. 2, lines 64-66).

Regarding claim 43, McAlear also discloses detecting the presence of a current flowing and identifying thereby (e.g., col. 2, lines 64-66).

Regarding claims 44 and 45, McAlear also discloses open and closed circuits (e.g., col. 2, lines 64-66).

Regarding claim 46, McAlear also discloses the length of wire (e.g., col. 2, lines 64-66, "current flowing").

Regarding claim 49, McAlear also discloses automatically identifying active ports (e.g., col. 2, lines 64-66).

Regarding claim 50, McAlear also discloses storing information relating to IDs (e.g., col. 3, lines 35-36).

Regarding claim 51, McAlear also discloses using active port information when performing sequencing operations on the ports where only selected active ports are sequenced (e.g., col. 3, lines 39-41).

3. *Claims 1, 13, 14, 25, 26, 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Bastiani (US 6675243).*

Regarding claim 1, Bastiani discloses automatically determining whether an external component is connected to the first port and identifying as active or inactive thereby (e.g., Figure 34; col. 33, lines 23-25), and distinguishing between active and inactive ports during control (e.g., col. 34, lines 16-17).

Regarding claim 13, Bastiani also discloses the computer program product of the parent claim (e.g., col. 6, lines 9-12).

Regarding claim 14, Bastiani discloses automatically identifying active ports, which are those with an external load physically connected (e.g., col. 33, line 37), and sequencing only desired active ports of the electronic device (e.g., col. 34, lines 16-17).

Regarding claim 25, Bastiani also discloses the computer program product of the parent claim (e.g., col. 6, lines 9-12).

Regarding claim 26, Bastiani discloses a processor and memory, the system configured or designed to automatically determine whether an external component is connected to the first port (e.g., col. 33, line 23-25), and the system designed to

distinguish between active and inactive ports during management (e.g., col. 34, lines 16-17).

Regarding claim 38, Bastiani discloses a processor and memory, a sequencing system configured or designed to automatically determine whether an external component is connected to the active ports (e.g., col. 33, line 23-25), and the system designed to sequence only active ports during management (e.g., col. 34, lines 16-17).

Claim Rejections - 35 USC § 103

4. Claims 2, 16, 27, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colmenero as applied in parent claims supra, in view of Biebl.

Colmenero does not expressly mention the particular means of detection such as a capacitive load; however this is disclosed by Biebl. Biebl discloses sensing capacitive load to automatically identify devices as active or inactive (e.g., Figure 4, "Integrator"). It would be obvious to combine Biebl with Colmenero because Biebl teaches a means to sense capacitive loads in systems where the active identification of lamps is necessary. A person would be motivated to use Biebl's teaching to enable practicing the invention of controlling light displays beyond the specific embodiment of resistive load circuits, which serve merely as the express embodiment of Colmenero's invention. Therefore it would be obvious to one of ordinary skill in the art to combine Biebl with Colmenero to obtain the claimed invention.

5. Claims 3, 5, 17, 19, 28, 30, 41, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colmenero as applied in parent claims in view of Allgood (US 5920266).

Regarding claims 3, 17, 28, and 41, Colmenero does not expressly mention the particular means of detection such as a resistive load; however, this feature is disclosed by Allgood. Allgood discloses a resistive load, which automatically identifies (e.g., col. 2, lines 50-54). It would be obvious to combine Allgood with Colmenero because Allgood teaches the advantages of deriving a sense signal based on an event of cable insertion to provide identification for a system, such as Colmenero where an identification is selected according to such an event in a modular cable insertion system. Therefore it would be obvious to one of ordinary skill in the art to combine Allgood with Colmenero to obtain the claimed invention.

Regarding claims 5, 19, 30, and 43, Colmenero does not expressly mention the use of current flowing as a means of detection; however, this feature is disclosed by Allgood. Allgood discloses a current flow, which automatically identifies the event (e.g., col. 2, lines 50-54). It would be obvious to combine Allgood with Colmenero because Allgood teaches the advantages of deriving a sense signal based on an event of cable insertion to provide identification for a system, such as Colmenero where an identification is selected according to such an event in a modular cable insertion system. Therefore it would be obvious to one of ordinary skill in the art to combine Allgood with Colmenero to obtain the claimed invention.

6. *Claims 4, 18, 29, 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biebl as applied in parent claims supra, in view of Watanabe (US 4396868).*

Regarding claims 4, 18, 29, 42, Colmenero does not expressly mention the particular means of detection such as a inductive load that would correspond to an inductive light device; however this is disclosed by Watanabe. Watanabe discloses sensing inductive load to automatically identify devices as active or inactive (e.g., col. 4, lines 62-67). It would be obvious to combine Watanabe with Colmenero because Watanabe teaches a means to sense inductive loads in systems where the active identification of lamps is necessary. A person would be motivated to use Watanabe's teaching to enable practicing the invention of controlling light displays beyond the specific embodiment of resistive load circuits, which serve merely as the express embodiment of Colmenero's invention. Therefore it would be obvious to one of ordinary skill in the art to combine Watanabe with Colmenero to obtain the claimed invention.

7. *Claims 11-12, 23-24, 36-37 and 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colmenero as applied to parent claims in view of common and widely known exemplars of display lighting, as further evidenced by Bruce (US 5957564).*

Regarding claims 11-12, 23-24, 36-37 and 47-48, Colmenero mentions display or decorative lights (e.g., col. 1, lines 28-32), but does not expressly mention the particular embodiment of electrolumiscent wire or light emitting diode; however, the Examiner

takes Official Notice that these are widely known exemplars of display lights in such systems as the display lighting of Colmenero. This is further evidenced by Bruce, who discloses controlling "light emitting devices" and mentions the common examples of LED and electroluminescent devices (e.g., col. 1, lines 54-62). It would be obvious to combine LED and electrolumiscent devices, which are seen to be standard light devices, with Colmenero because Colmenero provides for control of standard light devices. Therefore it would be obvious to one of ordinary skill in the art to combine the LED or electrolumiscent devices with Colmenero to obtain the claimed invention.

8. *Claims 13 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colmenero as applied in parent claims, in view of common and widely held knowledge of logical equivalence of hardware and software, as further evidenced by Tanenbaum (Structured Computer Organization).*

Regarding claims 13 and 25, Colmenero does not expressly mention a computer program product; however Examiner takes Official Notice that implementation of hardware methods of Colmenero as software is a manifestly obvious and widely known feature, as further evidenced by Tanenbaum. Tanenbaum, in the reference work, teaches the well-known mantra "hardware and software are logically equivalent" (p. 11). Therefore it would be obvious to one of ordinary skill in the art to implement the hardware methods of Colmenero as a computer program product.

9. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Colmenero as applied in claim 38, in view of common and widely used practice of sensing events to cause results in an electronic device, as further evidenced by Allgood.

Regarding claim 49, Colmenero discloses a means to identify active ports (e.g., col. 3, lines 19-22); but he does not expressly mention the claimed automatic identification, provided one interprets automatic identification to implicitly recite a form of sensing signal from the active port (the ambiguity in recitation forms the basis of the rejection under 35 USC 112(2) supra). However, the Examiner takes Official Notice that it is widely known to that inserting a plug or cable can be sensed in an electronic device when the electronic device is selectively operable based on the cable insertion which is in fact the nature of the cable insertion of Colmenero. This common feature is further evidenced by Allgood. Allgood discloses automatic identification of a cable (e.g., col. 2, lines 48-50). A person of ordinary skill in the art would be motivated to use the automatic identification sensing of Allgood, because Allgood teaches the well understood advantages and common practice of sensing cable insertion to provide a signaling means in an electronic device. Therefore, it would be obvious to one of ordinary skill in the art to combine common practice of sensing cable insertion in a device selective to the insertion with Colmenero to obtain the claimed invention.

Response to Arguments

10. Applicant's arguments filed 8/30/04 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that Colmenero does not disclose the claimed features "relating to automatic detection of active and/or inactive ports of a sequencer as defined" (p. 10); however, at the cited exemplary passage, Colmenero discloses: "it should be apparent that the result of receiving such a parallel input from another module along with the clock pulse from that module, is to cause shift register 40 to respond in the same way at the same time as the shift register in the other module" (col. 4, lines 30-34) cited supra against claim 1, and "a switch for selecting between an external clock source and a local clock pulse generator" (col. 3, lines 23-25), cited supra against claim 6. In these claims at least, no detection is cited, rather an "identifying" step for which Examiner deems Colmenero anticipatory wherein the switch supports said identification. The step is further limited in claims 2-5 as "in response to detection of"; however, these claims do not rely on an anticipatory interpretation of Colmenero.

Some consideration is given to the amended use of "automatically" in the identification step. The plain language definition of automatic requires a process that is not manual. A reading of the passage quoted supra make it clear that an automatic process is involved in setting the switch. Therefore, the addition of "automatically" fails to overcome the rejection using Colmenero. Again, the features introduced in claims 2-5 limit the notion of automatic identification; however, Colmenero is not applied in isolation against these claims.

Applicant further argues that Colmenero does not disclose "features relating to the sequencing of only a first portion of ports of the sequencer which have been identified" (p. 10); however that is precisely the role of the switch. Either the ports are sequenced or they are not according to the setting of the cited switch (quoted supra).

Regarding claim 1, Applicant argues that McAlear "represent[s] non-analogous art since the teachings of McAlear are directed to a technique for interfacing peripheral devices to computers" (p. 11); however the relationship of the prior art to the applicant's particular embodiment is not at issue here. It is incumbent upon the Examiner to interpret the claimed invention as reasonably broad as possible. McAlear discloses a sequencer which anticipates the broadly claimed sequencer of the Applicant:

By definition, a sequencer is "a device for arranging in a sequence" and it must be determined whether McAlear discloses such a device, of course in addition to other elements of the claim. McAlear discloses the polling operation of the USB ports, for example, McAlear discloses "[t]he end hub 80 also performs some traditional USB hub functions, such as detecting the connection and disconnection of USB devices 100 to its USB ports 700. As with a conventional use of the USB protocol, the end hub 80 is periodically polled by the LAN hub 10 to report any change of the status of the USB ports 700" (col. 30, line 66 – col. 31, line 4). It is determined that the USB polling operation discloses a sequencing operation, and hence the claimed sequencer.

Thus the rejection of McAlear is maintained.

Regarding claim 1, Applicant argues that Bastiani does not disclose "features relating to automatic detection of active and/or inactive ports of a sequencer" (p. 12);

however, Bastiani discloses: "[a]n ASP device may be attached or detached from the ASP" (col. 33, lines 23-24) which is deemed anticipatory of the broadly claimed "automatically identifying the first port as an active port" and "automatically identifying the first port as an inactive port".

Applicant further argues that Bastiani does not disclose "the feature relating to the sequencing of only a first portion of ports of the sequencer which have been identified as active ports" (p. 12); however Bastiani discloses: "Once the host has determined that a device is attached, the host needs to set up the link to the device" (col. 34, lines 16-17), which is deemed to sequencing only a first portion; that is, the attached or "active" ports of the device, and is thus deemed anticipatory of the claimed invention.

In particular, consideration has been given as to whether the feature of sequencing, as claimed for example in claim 1, is found in Bastiani. Bastiani discloses, "[a]ccordingly, as ASP devices 106 are removed, the host interface detects that they are non-responsive and removes them from the polling list" (col. 8, lines 60-62). As in the case of McAlear, it is similarly determined that the polling operation as disclosed by Bastiani anticipates the sequencing as it is claimed.

Thus the rejection using Bastiani is maintained.

It is determined that sequencing is not a feature of Biebl, therefore the rejection of Biebl is withdrawn in light of the amended claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

Khanh Dang
Primary Examiner